Abstract of the Disclosure

Semiconductor devices and methods for fabricating the same include a device isolation layer formed at a predetermined region of a semiconductor substrate to define a cell active region, a resistor active region, and an MROM active region. The device further includes a floating junction region, a resistive junction region, and a channel junction region, which are formed in the cell active region, the resistor active region, and the MROM active region, respectively. The floating junction region, the resistive junction region, and the channel junction region have the same thickness. A covering gate and an MROM gate cross over the resistive active region and the channel active region, respectively. Also, a memory gate and a select gate cross over the cell active region. The method includes forming a device isolation layer at a predetermined region of a semiconductor substrate to define a cell active region, a resistor active region, and an MROM active region. A floating junction region, a resistive junction region, and a channel junction region are then formed in the cell active region, the resistor active region, and the MROM active region, respectively. Thereafter, a select gate and a memory gate are formed on the cell active region. Also, a covering gate and an MROM gate are formed on the resistor active region and the MROM active region, respectively. The floating junction region, the resistive junction region, and the channel junction region are preferably formed at the same time.

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